

REMARKS

Claims 1-4, 6-12 and 33-44 are pending in the present application. Applicant notes with appreciation the indication of allowable subject matter with respect to claims 8, 10, 11 and 38-44. With entry of this Amendment, Applicant amends claims 1, 2 and 6 and adds new claims 45 and 46. Reexamination and reconsideration are respectfully requested.

Request for Correction of Inventorship

Claims 13-32 were cancelled without prejudice in the previous response to the restriction requirement. As a result of the cancellation of the claims, it is requested that the inventorship of the present application be corrected to delete Tokio SHIRAKAWA as an inventor pursuant to 37 C.F.R. § 1.48(b)(1). A processing fee set forth in § 1.17(i) is to be charged to deposit account below and pursuant to the accompanying fee transmittal.

Abstract

The Examiner objected to the Abstract for exceeding 150 words. Applicants have amended the Abstract to be less than 150 words. Accordingly, Applicants respectfully request that the Examiner withdraw the objection.

Rejection under § 102(b)

The Examiner rejected claims 1-3, 6, 7, 9, 33 and 34 under 35 U.S.C. § 102(b) as being anticipated by Suzuki et al. (U.S. Patent No. 5,489,746). The rejection is respectfully traversed as set forth below for each claim.

Claim 1

The present invention as set forth in claim 1 is directed to a compressed data structure for storing a plurality of samples of compressed waveform data. Claim 1 has been amended in two ways. First, it recites that "irrespective of the number of bits per sample of compressed waveform

data stored in said data area of each frame, each frame is stored over said predetermined number j of successive addresses.” Second, claim 1 recites “wherein said auxiliary information area and data area in each frame are fixed in position irrespective of the number of bits per sample of compressed waveform data stored in the frame.”

Support for these two recitations are found throughout the specification and drawings. For example, Fig. 8 shows, in the first illustrated structure, a frame of data storing samples of two bits. The data is stored over 5 addresses of memory from “00” to “04.” Each address has a data width of 16 bits (indicated by the hash marks at the top) for total of 80 bits per frame (i.e., 5 addresses X 16 bits). A 20-bit area from address 00 to address 01 stores auxiliary information. The remainder 60-bit area stores 30 data samples of two bits.

Fig. 8 further shows the data structure for frames of data storing samples at 3 bits, 4 bits, 5 bits, 6 bits and 10 bits. Note that irrespective of the number of bits per sample, each frame is stored over a predetermined number of addresses, i.e., five addresses. Thus, while the number of samples per frame may change – e.g., 30 samples in the case of the frame storing samples of 2 bits while 6 samples in the case of the frame storing samples of 10 bits – each frame is stored over five addresses. Moreover, note that auxiliary information area and the data area for each illustrated frame is fixed in position. Whether the frame stores samples of 2 bits or 10 bits, the auxiliary information area ends at a position in address 01 in each frame.

In contrast, the ‘746 Patent does not disclose the above two recitations. The ‘746 Patent discloses a data structure in which the number of bits per sample is variable per frame, but the number of samples per frame is fixed. For example, as illustrated in Fig. 2, “Frame 0” has samples of 11 bits, and “Frame 1” has samples of 10 bits. Each frame, however, has the same number of samples, i.e., 16. Thus, the size of the data area for each frame is variable. In the case of “Frame 0,” the data area is 176 bits (16 samples X 11 bits). In the case of “Frame 1,” the data area is 160 bits (16 samples X 10 bits).

Because the size of the data area varies between the frames, the ‘746 Patent fails to disclose the above two recitations. First, it fails to disclose “wherein irrespective of the number of

bits per sample of compressed waveform data stored in said data area of each frame, each frame is stored over said predetermined number j of successive addresses.” The variable size of the data areas between “Frame 0” and “Frame 1” precludes each frame from being stored over a predetermined number of addresses. Moreover, the variable size of the data areas also precludes that “said auxiliary information area and data area in each frame are fixed in position irrespective of the number of bits per sample of compressed waveform data stored in the frame.”

Accordingly, Applicant respectfully submits that claim 1 is not anticipated by the ‘746 Patent.

Claim 2

Claim 2 has been amended to recite that “wherein said data area ranges over a plurality of addresses in the j successive addresses irrespective of the number of bits per sample of the compressed waveform data stored in the data area of each frame.”

The ‘746 Patent does not disclose this recitation. The ‘746 Patent discloses frames having a variable number of bits per sample, such as 11 bits or 10 bits, but a fixed number of samples per frame. As a result, the address range in a memory where the data area is located is variable based on the number of bits per sample for each frame.

In rejecting claim 2, the Examiner cited Fig. 2 as disclosing the “data area ranges over a plurality of addresses in the j successive addresses” However, Fig. 2 illustrates the number of samples per frame and not the memory address.

Accordingly, Applicant respectfully submits that claim 2 is not anticipated by the ‘746 Patent.

Claim 3

Applicant respectfully submits that claim 3 is not anticipated by the ‘746 Patent for at least the reasons set forth above with respect to claim 1.

Claim 6

Claim 6 is directed to a waveform storage processing apparatus. It recites a framing section wherein "each of the frames has a fixed total number of bits and includes a fixed auxiliary information and a remaining data area." Claim 6 has been amended to recite "wherein irrespective of the number of bits per sample of compressed waveform data stored in said data area of each frame, each frame is stored over said predetermined number j of successive addresses."

The '746 Patent fails to disclose either recitation. As illustrated in Fig. 2, the number of bits per sample is variable per frame, but the number of samples is the same per frame. The size of the data area for each frame is accordingly variable. "Frame 0" has a data area of 176 bits (16 samples X 11 bits), while Frame 1 has a data area of 160 bits (16 samples X 10 bits). Thus, the '746 Patent fails to disclose that "each of the frames has a fixed total number of bits and includes a fixed auxiliary information area and a remaining data area."

Moreover, the variable size of the data areas between the frames precludes that each frame is "stored over a predetermined number j of successive addresses" irrespective of the number of bits per sample.

Accordingly, claim 6 is not anticipated by the '746 Patent.

Claim 7

Applicant respectfully submits that claim 7 is not anticipated by the '746 for at least the reasons set forth above with respect to claim 1. Additionally, Applicant notes that the Examiner's citation to Fig. 2 as disclosing the recitation of claim 7 is without support. Fig. 2 illustrates the number of samples per frame and does not disclose that " m bits of the n bits (where $m < n$) in the j addresses of said memory contain said data area, and a remaining ' $n-m$ ' bits of the n bits in the j addresses of said memory contain said auxiliary information area."

Claims 9, 33 and 34

Applicant respectfully submits that these claims are not anticipated by the '746 Patent for at least the reasons set forth above with respect to claim 1 from which claims 33 and 34 depend and with respect to claim 7 from which claim 9 depends.

Rejection under § 103(a)

The Examiner rejected claims 4 and 35-37 as being unpatentable over the '746 Patent in view of Suzuki et al. (U.S. Patent No. 5,831,193). The rejection is respectfully traversed. The '193 Patent relates to varying the sampling frequency of waveform data in time and was merely cited for its alleged disclosure of an address generation section. Thus, it is believed that the '193 Patent does not make up for the deficiencies of the '746 Patent as discussed above and that claims 4 and 35-37 are patentable over the '746 Patent and the '193 Patent.

Claims 12, 45 and 46

In the previous response to the restriction requirement, the Applicant traversed the restriction of claim 12. In the present Office Action, the Examiner has maintained his restriction of claim 12. Applicant respectfully requests that the Examiner reconsider his restriction and include claim 12 within the present examination.

Claim 12 is directed to a waveform storage processing apparatus. The apparatus comprises a writing section that writes data to a "predetermined number j of successive addresses of said storage section" for each frame. This recitation is similar to a recitation in claim 1 which is directed to a data structure. Moreover, it defines m bits of data and n-m bits of auxiliary information. This recitation is similar to the recitation of claim 7 which depends from claim 1. Accordingly, the Examiner's search for prior art relating to the data structure of claims 1 and 7 will include a search for an apparatus that writes data in the manner claimed in claim 12. It is thus believed that the burden on the Examiner in examining claim 12 with claims 1 and 7 is not serious. Applicant therefore respectfully requests that the Examiner reconsider the restriction of claim 12 and

examine it with the pending claims. To highlight the similarity of claim 12 to claim 1, Applicant has added two new claims depending from claim 12 that define the auxiliary information area and the data area as well as that the number of bits per sample are variable.

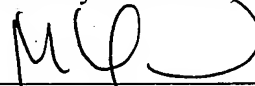
If, for any reason, the Examiner finds the application other than in condition for allowance, Applicant requests that the Examiner contact the undersigned attorney at the Los Angeles telephone number (213) 892-5630 to discuss any steps necessary to place the application in condition for allowance.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. 393032041500.

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Respectfully submitted,

By



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